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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,269	02/25/2004	Chien-Ping Huang	58102-DIV (71987)	5161

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,269	HUANG, CHIEN-PING	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-23,25-32,34-40 and 42-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-23,25-32,34-40 and 42-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/211,430.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Request for Continued Examination filed on 8/18/06 is acknowledged.

2. The cancellation of claims 1-15, 24, 33 and 41 in Paper filed on 8/18/06 is acknowledged.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 29-32, 35-40, and 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al (US. 6,580,167) in view of Applicant's admitted prior art.

Regarding claims 29-30 and 38, Glenn (Figs. 1-3) discloses a heat dissipating structure for a semiconductor package 100 having a plurality of bonding wires 112, comprising: a flat portion 133 having a top surface and a bottom surface opposed to the top surface, wherein at least a peripherally-situated recess 140 is formed on the top surface of the flat portion; and a plurality of support portions 152 formed at edge corners of the bottom surface of the flat portion 133 (Fig. 1), wherein the support portions 152 are arranged to form a space between two adjacent support portions 152, and the space is dimensioned to have a predetermined height larger than a height of wire loops of the bonding wires 112 (see Fig. 3).

Glenn does not disclose a passive component mounted on the substrate 102.

However, Applicant's admitted prior art (Fig. 5) teaches a semiconductor package having a chip 31, and passive components disposed on the substrate 30 (not shown, see Applicant's specification, page 2, lines 11-13). Accordingly, it would have been obvious to form passive components on the substrate of Glenn in order to provide a semiconductor package having a desired circuitry, which is required by the electronic applications.

Regarding claims 31-32, 39 and 40, Glenn's Fig. 2 further discloses that a protrusion 138 is formed on the bottom surface of the flat portion and the top surface 130U of the flat portion is exposed to outside of the package.

Regarding claims 35-37 and 43-45, Glenn further discloses that each of the support portions 152 has one end E1 attached to the flat portion and the other end E2 formed with a contact portion 154A (see Figs. 1 and 2), the contact portion 154A extends laterally with respect to the flat portion and has a rectangular shape (see Fig. 1).

5. Claims 34 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al and AAPA as applied to claims 29 and 38 above, and further in view of Tang et al (US. 6,246,115).

Neither Glenn nor AAPA discloses that a hole is formed in each of the support portions.

However, Tang (Figs. 2 and 3) teaches a heat dissipating structure having a plurality of support portions 321, each of the support portions 321 is formed with a hole 321a for allowing an encapsulating resin 33 to pass through the hole. Accordingly, it

would have been obvious to modify the heat dissipating structure of Glenn by forming a hole in each of the support portions 152 because such holes would help enforce the bonding between the heat dissipating structure and the encapsulating resin, as taught by Tang (column 5, lines 5-8).

6. Claims 16-23 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al (US. 6,580,167) in view of AAPA and Chiang et al (US. 5,736,785).

Regarding claims 16 and 19, Glenn (Figs. 1-3) discloses a heat dissipating structure for a semiconductor package 100 having a substrate 102, a chip 104 mounted on the substrate and electrically connected to the substrate via a plurality of conductive elements 112, the heat dissipating structure comprising: a flat portion 133, wherein at least a peripherally-situated recess 140 is formed on a top surface of the flat portion; and a plurality of support portions 152 formed at edges of the flat portion for supporting the flat portion in position above the chip (see Fig. 1), wherein the support portions 152 are mounted at a predetermined area on the substrate 102 and free of interference with an arrangement of the chip 104 and the conductive elements 112, and the support portions 152 are arranged to form a space between two adjacent support portions 152, the space being sufficient dimensioned to accommodate the conductive elements 112.

Glenn does not disclose a passive component mounted on the substrate 102.

However, Applicant's admitted prior art (Fig. 5) teaches a semiconductor package having a chip 31, and passive components disposed on the substrate 30 (not shown, see Applicant's specification, page 2, lines 11-13). Accordingly, it would have

been obvious to form passive components on the substrate of Glenn in order to provide a semiconductor package having a desired circuitry, which is required by the electronic applications.

Neither Glenn nor AAPA discloses the conductive elements 112 passing through the space to reach an area on the substrate 102 outside coverage of the heat dissipating structure.

However, Chiang (Figs. 4A and 4C) teaches a heat dissipating structure having the conductive elements 108 (i.e., wires) passing through the space to reach an area on the substrate 104 outside coverage of the heat dissipating structure (Fig. 4C). Accordingly, it would have been obvious to pass the conductive elements or wires 112 of Glenn through the space to reach an area on the substrate outside coverage of the heat dissipating structure in order to provide the electrical interconnections to the conductive traces formed on the substrate area outside coverage of the heat dissipating structure, as taught by Chiang's Fig. 4C.

Regarding claims 17-18, Glenn further discloses that the conductive elements 112 are bonding wires, a further discloses that the conductive elements 112 are bonding wires, a plurality of bond fingers 110 are formed on the substrate 102 for allowing the bonding wires 112 to be bonded to the bond fingers 110, and the flat portion 133 above the chip 104 by the support portions 152 and forms a predetermined height larger than a height of wire loops of the bonding wires 112 (see Fig. 2).

Regarding claims 20-23, Glenn further discloses that: the support portions 152 are situated at edge corners of the flat portion 133 (Fig. 1), the flat portion has a top

surface 130U exposed to outside of the encapsulant 160 (Fig. 2) and a bottom surface being formed with the support portions 152, the chip 104 and the conductive wire elements 112 are encapsulated by an encapsulant 160, and a protrusion 138 is formed on the bottom surface of the flat portion and extends toward the chip 104.

Regarding claims 26-28, Glenn further discloses that each of the support portions 152 is formed with a contact portion 154 at a position in contact with the substrate 102, the contact portion 154 extends laterally with respect to the substrate 102 and has a rectangular shape (Fig. 1).

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn, AAPA and Chiang as applied to claim 16 above, and further in view of Tang et al (US. 6,246,115).

Neither Glenn nor Chiang discloses that a hole is formed in each of the support portions.

However, Tang (Figs. 2 and 3) teaches a heat dissipating structure having a plurality of support portions 321, each of the support portions 321 is formed with a hole 321a for allowing an encapsulating resin 33 to pass through the hole. Accordingly, it would have been obvious to modify the heat dissipating structure of Glenn by forming a hole in each of the support portions 152 because such holes would help enforce the bonding between the heat dissipating structure and the encapsulating resin, as taught by Tang (column 5, lines 5-8).

Response to Arguments

8. Applicant's arguments with respect to the claimed invention have been considered but are moot in view of the new ground(s) of rejection.

The new references are applied in the new ground of rejections.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC
September 14, 2006

PHAT X. CAO
PRIMARY EXAMINER